Reachability Analysis of Closed-Loop Switching Power Converters

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Background

Modeling

Analysis

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Switching Power Converters

- 1. DC-DC Converters
 - Buck converter
 - Boost converter
 - Buck-Boost converter
- 2. Rectifiers (AC-DC)
- 3. Inverters (DC-AC)
- 4. Transformers

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Buck Converter

Circuit Diagram

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Design Verification of Switching Power Converters

- 1. Traditional simulation methods
 - Simulink/Stateflow
 - PSpice
 - Monte Carlo
- 2. Hybrid system verification tools
 - SpaceEx

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SpaceEx

Software Architecture



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SpaceEx Reachability Algorithm

- Symbolic States
- Control:
 - 1. Maximum iterations
 - 2. Relative and absolute error

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SpaceEx Interface

Setting Maximum Iterations and Relative and Absolute Errors

Model Specifica	tion Options Output Advanced	
Scenario	LGG Support Function	?
Directions	🛇 box 💿 oct 🔘 uni	2
Clustering percentage	100	2
Aggregate sets	Convex hull	3
Sampling time	0.00001	2
Flowpipe tolerance	0.001	2
Initial samples	50	3
Local time horizon	1	3
Max. iterations	15	2

Model	Specifica	tion	Options	Output	Advanced	
Relative erro	or	1.0e	e-12			0
Absolute en	ror	1.0e	e-15			0
ODE toleran	ce rel.					
ODE toleran	ce abs.					
Additional o	ptions					0
						1
SpaceEx Ve	rsion	Spac v0.9 13:1	eEx State .7beta, co 6:57, 64-b	Space Ex mpiled No oit float, 64	plorer, v 26 2012, 4-bit precise	float
Interface V	ersion	Spac v1.0	eEx Web -BETA1.4	Interface // 2011-1)-24	
3D Display li	brary	www	v.javaview	.de		

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SpaceEx Interface

Initial States and Output Specification

Mode	Specification	Options	Output	Advanced	
System	buck	▼ Upd	ate		0
• buck					
Contro	olled : il, vc, t, gt				
Const	ant-Dynamics : vs, v	rref, delta, tma	ix.		
- Basero	components : buck_	template_1			
Initial state	s				3
loc(buck_t == 0 & vs=	emplate_1)==ch =12 & tmax ==0.0	arging & il : 001 & vref=	== 0 & vc = =5 & delta:	=0 & t == 0 8 ==0.1	gt
					1
Forbidden s	states				/

Model Specification Op	ions Output Advanced
Output format 2D (ge) 🔽 🚷
Output variables i1, vo	gt 🦉
Output error	0
Generate PDF file	
Echo the generated command l	nes to the console 📃
Verbosity Debug	4 💌 🔞

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Model of Open-Loop Configuration

$$x = \begin{bmatrix} i_L \\ V_c \end{bmatrix}$$
$$A_o = A_c = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$$
$$B_c = \begin{bmatrix} 1/L \\ 0 \end{bmatrix} V_s \text{ or } B_o = \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_s$$

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Block Diagram



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System Model

$$A_{ctrl} = \begin{bmatrix} -\frac{1}{p_1} & 0 & 0 \\ -\frac{p_2}{p_1 p_3} + \frac{1}{p_3} & -\frac{1}{p_3} & 0 \\ -\frac{p_2 p_4}{p_1 p_3 p_5} + \frac{p_4}{p_3 p_5} & \frac{-p_4}{p_3 p_5} + \frac{1}{p_5} & 0 \end{bmatrix}$$
$$x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} \quad B_{ctrl} = \begin{bmatrix} \frac{1}{p_1} \\ \frac{p_2}{p_1 p_3} \\ \frac{p_4 p_2}{p_1 p_3 p_5} \end{bmatrix}$$

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Composed System

$$\dot{x} = A_c \cdot x_c + B_{comp} \left(V_{ref} - V_{out} \right)$$

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Composed System



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Hysteresis Controller

Hybrid Model of Buck Converter and Hysteresis Controller



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Results of Hysteresis Controller

Capacitor Voltage vs. Global Time



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Results of Hysteresis Controller

Inductor Current vs. Global Time



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Simulink Results for Composed System

Simulink Model



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Simulink Results for Composed System



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Simulink Results for Composed System

Capacitor Voltage vs. Global Time



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Conclusion and Future Work

- Open-loop and hysteresis controller configurations
- Modeling flexibility
- Overapproximation issues

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